IN THE CLAIMS

Please amend the claims to be in the form as follows:

Claim 1 (currently amended): A transmission system comprising at least a station of a first type and a station of a second type which include a transmitting part having a transmit timing controller for transmitting data at a transmit timing and a receiving part having synchronizing circuits for synchronization with data transmitted from different station types to provide a receive timing, characterized in that the transmit timing is fixed in response to the receive timing ~~characterized~~ and in that the receiving part of the station of the second type has a synchronization circuit that provides chip fractions shifted in time that are used to modify frequencies of data received from the first station type.

Claim 2 (currently amended): A transmission system as claimed in Claim 1, formed by a station of the first type where the receiving part comprising a synchronizing circuit for determining the receiving timing of a plurality of stations of the second type, characterized in that the synchronizing circuit of the station of the first type is ~~known~~ compatible to all the stations of the second type.

Claim 3 (previously presented): A transmission system as claimed in Claim 1 characterized in that the stations of the second type comprise means for evaluating a frequency shift, of the receiving frequency relative to the transmitting frequency of the station of the first type and means for modifying the transmitting frequency of the station of the second type as a function of this frequency deviation.

Claim 4 (currently amended): A transmission system comprising at least a station of a first type and a station of a second type which include a transmitting part having a transmit timing controller for transmitting data at a transmit timing and a receiving part having synchronizing circuits for synchronization with data transmitted from different station types to provide a receive timing, characterized in that the receiving part of the station of the second type has a synchronization circuit that provide chip fractions shifted in time that are used to modify frequencies of data received from the first station type and the station of the first type comprises

a receiving circuit to be shared by all the stations of the second type to which it is connected.

Claim 5 (currently amended): A synchronization method suitable for a system comprising at least a station of a first type and a station of a second type which include a transmitting part having a transmit timing controller for transmitting data at a transmit timing and a receiving part having synchronizing circuits for synchronization with data transmitted from different station types to provide a receive timing, characterized in that it comprises the following steps:

- providing the receiving part of the station of the second type with a synchronization circuit that generates chip fractions shifted in time,
- measuring the receive clock derivation made at the stations of the second type,
- ~~comparing~~ adjusting the transmit clock at the station of the second type by adopting the opposite deviation value,
- ~~single~~ synchronization of the receive clock at the station of the first type.

Claim 6 (previously presented): A transmission system as claimed in Claim 1, wherein the synchronization circuit provides chip fractions shifted in time produces a first output corresponding to a satisfactory state of synchronism.

Claim 7 (previously presented): A transmission system as claimed in Claim 6, wherein the synchronization circuit provides chip fractions shifted in time produces an already produced chip fraction output that contains chip fraction previously produced at the first output.

Claim 8 (previously presented): A transmission system as claimed in Claim 7, wherein the synchronization circuit provides chip fractions shifted in time produces a recently produced chip fraction output that contains chip fraction that have just been produced.

Claim 9 (currently amended): A transmission system as claimed in Claim 8, wherein the receiving part of the station of the second type further comprises an analysis circuit that receives chip fractions shifted in time by the synchronization circuit and determines ~~a~~ the frequency drift, therefrom.

Claim 10 (previously presented): A transmission system as claimed in Claim 9, wherein the receiving part of the station of the second type further comprises means for modifying clock frequencies in response to the frequency drift.

Claim 11 (previously presented): A transmission system as claimed in Claim 4, wherein the synchronization circuit provides chip fractions shifted in time produces a first output corresponding to a satisfactory state of synchronism.

Claim 12 (previously presented): A transmission system as claimed in Claim 11, wherein the synchronization circuit provides chip fractions shifted in time produces an already produced chip fraction output that contains chip fraction previously produced at the first output.

Claim 13 (previously presented): A transmission system as claimed in Claim 12, wherein the synchronization circuit provides chip fractions shifted in time produces a recently produced chip fraction output that contains chip fraction that have just been produced.

Claim 14 (previously presented): A transmission system as claimed in Claim 13, wherein the receiving part of the station of the second type further comprises an analysis circuit receives chip fractions shifted in time by the synchronization circuit and determines a frequency drift, therefrom.

Claim 15 (previously presented): A transmission system as claimed in Claim 14, wherein the receiving part of the station of the second type further comprises means for modifying clock frequencies in response to the frequency drift.

Claim 16 (previously presented): A method as claimed in Claim 5, wherein the synchronization circuit provides chip fractions shifted in time produces a first output corresponding to a satisfactory state of synchronism.

Claim 17 (previously presented): A method as claimed in Claim 16, wherein the synchronization circuit provides chip fractions shifted in time produces an already produced chip fraction output

that contains chip fraction previously produced at the first output.

Claim 18 (previously presented): A method as claimed in Claim 17, wherein the synchronization circuit provides chip fractions shifted in time produces a recently produced chip fraction output that contains chip fraction that have just been produced.

Claim 19 (previously presented): A method as claimed in Claim 18, wherein the receiving part of the station of the second type further comprises an analysis circuit receives chip fractions shifted in time by the synchronization circuit and determines a frequency drift, therefrom.

Claim 20 (previously presented): A method as claimed in Claim 19, wherein the receiving part of the station of the second type further comprises means for modifying clock frequencies in response to the frequency drift.